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Realization of Boolean Logic Functionality Using Redox-Based Memristive Devices

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Emerging resistively switching devices are thought to enable ultradense passive nanocrossbar arrays for use as random access memories (ReRAM) by the end of the decade, both for embedded and mass storage applications. Moreover, ReRAMs offer inherent logic-in-memory (LIM) capabilities due to the nonvolatility of the devices and therefore great potential to reduce the communication between memory and calculation unit by alleviating the so-called von Neumann bottleneck. A single bipolar resistive switching device is capable of performing 14 of 16 two input logic functions in the logic concept presented by Linn et al. ("CRS-logic"). In this paper, five types of selectorless devices are considered to validate this CRS-logic concept is experimentally by means of the IMP and AND logic operations. As reference device a TaO_x-based ReRAM cell is considered, which is compared to three more advanced device configurations consisting either of a threshold supported resistive switch (TS-ReRAM), a complementary switching device (CS), or a complementary resistive switch (CRS). It is shown that all of these devices offer the desired LIM behavior. Moreover, the feasibility of XOR and XNOR operations using a modified logic concept is applied for both CS and CRS devices and the pros and cons are discussed.

1. Introduction

Redox-based resistive memories (ReRAM) are highly attractive candidates for realization of future ultradense passive crossbar memories.[1] Both, valence change memories (VCM) and electrochemical metallization cells (ECM) offer excellent endurance,[2,3] retention,[4,5] and scaling properties.[6,7] Implementing those devices as junctions of passive crossbar arrays enables $4F^2$ passive crossbar arrays, which lead to ultimately scalable memories.[8] Furthermore, due to the nonvolatility of the devices, logic operations within the array are feasible.[9,10]

Basically, one can distinguish two approaches for realization of digital logic functionality. In the first approach, ReRAM devices are used as switchable interconnects, enabling a field programmable gate arrays-like structures,[11–14] look-up tables (LUTs),[15] or content addressable memories.[16,17] In the second approach, ReRAM devices themselves are performing the logic operation, either in a sequential[18–22] or combinational manner.[23,24] The later one tries to resemble conventional logic gates with memristive devices and requires no dedicated number of steps but is by principle not compatible to ultradense $4F^2$ passive crossbar arrays. In 2012, we theoretically derived an advanced sequential logic concept, called CRS-logic, which reduces the device count and number of steps substantially.[25]

In general, sequential logic enables computations directly in the memristive array and so the communication overhead between arithmetic logic unit and memory is avoided, also known as von Neumann bottleneck. In fact, cross-point junction devices can be considered as elementary processing units for performing logic operations, using bipolar resistive switches (BRS, ECM, or VCM devices).[18,25] Also unipolar resistive switches, e.g., phase change memory devices can be used for logic operations[26] but are not part of this investigation.

However, building large-scale arrays from basic ReRAM devices could lead to dramatic parasitic currents.[27] To overcome this issue a certain select paradigm must be implemented. The straight forward approach is the addition of a serial selector to each cross-point junction device,[28] but the implementation is challenging due to the current density requirements for the bipolar rectifying selector. However, alternative selectorless approaches also exist: The first one relies on ReRAM devices offering an intrinsic ON-state nonlinearity[29,30] or rather a threshold switching behavior, i.e., TS-ReRAM.[31] A second concept uses a complementary resistive switch (CRS), i.e., two antiserially connected bipolar switching

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devices, at each cross-point junction.[27] A derivate concept uses special ReRAM cells offering complementary switching (CS) inherently.[32] Recently, the CRS-logic concept[25] was proven by means of memristive simulations,[33,34] and first experimental results confirmed these findings using a VCM-based CRS device.[35] In this work we prove by means of electrical measurements that the CRS-logic concept works properly for the following types of selectorless crossbar junctions: 1) basic VCM ReRAM cells (BRS-VCM), 2) ReRAM cells with intrinsic threshold switching (TS-ReRAM), 3) VCM complementary resistive switches (CRS-VCM), 4) ECM complementary resistive switches (CRS-ECM), and 5) ReRAM cells offering complementary switching (CS-VCM). Moreover, we demonstrate experimentally that CS and CRS devices can adopt the logic concept of You et al.[36]

2. Devices

For each type of selectorless crossbar junction an exemplary device has been fabricated. The corresponding device stacks are depicted in **Figure 1**a–e. As the basic VCM ReRAM cell a bipolar switching VCM-type Pt/TaO_x/Ta/Pt device is considered (BRS-VCM) (Figure 1a) and a Pt/NbO_x/Ti/Pt stack is investigated as a threshold supported ReRAM device (Figure 1b). For complementary restive switches both, a VCM-type Pt/TaO_x/Ta/TaO_x/Pt[35] (Figure 1c) and an ECM-type Pt/Ag/GeS_x/Pt/GeS_x/Ag/Pt[37] cell, are considered (Figure 1d). Note that the first one is a fully integrated CRS device whereas the latter one is fabricated laterally. Finally, a VCM-type Pt/TaO_x/Ta/Pt (Figure 1e) serves as CS device, which offers different layer thicknesses compared to the stack in Figure 1a.

Typical *I*–*V* characteristics of these devices are depicted in **Figure 2**a–c. In Figure 2a, the *I*–*V* characteristic of a generic bipolar resistive switching device is depicted. Starting from a high resistive state (HRS), the ReRAM cell switches to the low resistive state (LRS) for positive input voltages after reaching V_{Set}. The RESET operation occurs for negative voltages at V_{Reset}. We define the device state HRS as Z = '0' (blue cube) and the LRS as Z = '1' (yellow cylinder). In Figure 2b the *I*–*V* characteristic of a ReRAM device offering inherent threshold switching is depicted. Note that a similar *I*–*V* characteristic is obtained for a ReRAM device plus serially added threshold switch.[31] If the ReRAM device is in the HRS initially, a relatively large voltage $V_{R,Set}$ for the SET of the ReRAM and a subsequent TS turn ON is required. In contrast, the TS alone would turn ON shortly after reaching $V_{TS,1}$ if the memory element is in the LRS. During the decline of the positive voltage the TS turns OFF at $V_{TS,1}$, while the memory stays in the LRS. For negative voltages and the memory element in LRS the TS turns ON again at $V_{TS,2}$. When reaching $V_{R,Reset}$ the memory element switches back to HRS, i.e., the current decreases and the TS inherently also turns OFF. As for basic ReRAM cells, we define the ReRAM state HRS as Z = '0' (blue cube) and LRS as Z = '1' (yellow cylinder). In Figure 2c, a generic *I*–*V* characteristic of a CRS or CS device is depicted. A CRS device consists of two bipolar switching devices A and B, whereas a CS device has two interfaces A and B, that are either in an LRS or an HRS.[27,38] CRS devices and CS devices offer three states: A:LRS/B:HRS (Z = '0', blue cube), A:HRS/B:LRS (Z = '1', yellow cylinder), and A:LRS/B:LRS (only relevant for read-out). Starting from LRS/HRS, the CRS cell switches to LRS/LRS at $V_{th,1}$ and further to HRS/LRS at $V_{th,2}$. Similarly, for negative voltages the CRS cell switches to LRS/LRS at $V_{th,3}$ and back to LRS/HRS at $V_{th,4}$.

3. Sequential Logic Concept

The first ReRAM-based sequential logic concept was introduced by Borghetti and co-workers.[18] In contrast to combinational logic, sequential logic requires several steps and an external CMOS-based logic-in-memory (LIM) controller. In the case of Borghetti's concept this LIM has to control at least two ReRAM memory elements for each elementary logic function. In the CRS-logic only one device is required to perform 14 of 16 two input Boolean logic functions in one to three steps.[25] Details can be found in Table S1 (Supporting Information). In **Figure 3**a, the corresponding finite state machine is depicted. In general, each junction element is considered as a two terminal device (terminals T1 and T2) at which the input logic signals are applied. The logical '1' is represented by a high potential (V) whereas a low potential (ground (GND)) represents a logical '0', Depending on the previous device state Z' the junction is only switched for a certain input combination of T1 (top electrode, TE) and T2 (bottom electrode, BE) (e.g., '01' means T1 = '0' and T2 = '1'), leading to the basic function for the state Z:

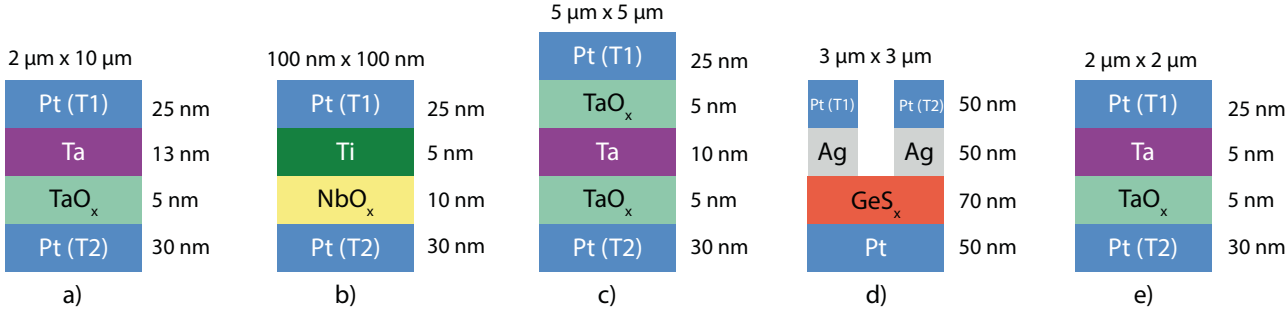

Figure 1. Material stacks of the considered devices. a) BRS-VCM (Pt/TaO_x/Ta/Pt stack), b) TS-ReRAM (Pt/NbO_x/Ti/Pt stack), c) CRS-VCM (Pt/TaO_x/Ta/TaO_x/Pt), d) CRS-ECM (Pt/Ag/GeS_x/Pt/GeS_x/Ag/Pt), and e) CS-VCM (Pt/TaO_x/Ta/Pt). Details of the fabrication can be found in the Experimental Section. T1 and T2 define the two terminals that are used in the electrical measurements.

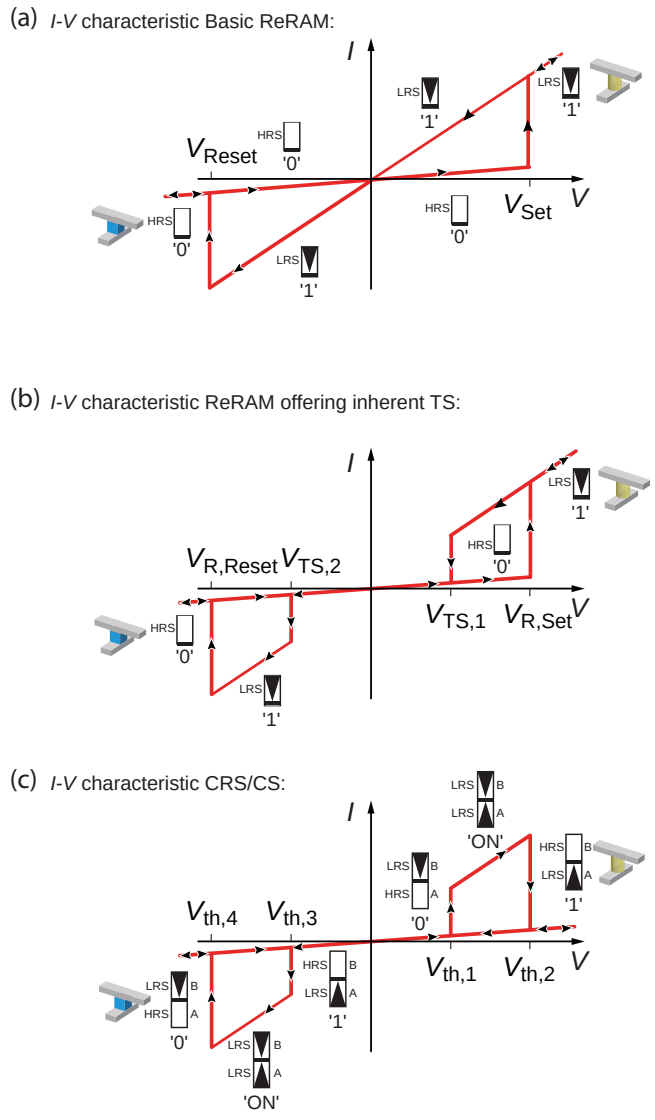

Figure 2. The *I–V* characteristics of a) a generic bipolar resistive switching device, b) a ReRAM device offering inherent threshold switching, and c) a CRS or CS device. The arrows indicate the run of the curve and the marked voltages the switching voltages.

$$Z = (\text{T1 RIMP T2}) \cdot (Z') + (\text{T1 NIMP T2}) \cdot (\text{not } Z') \quad (1)$$

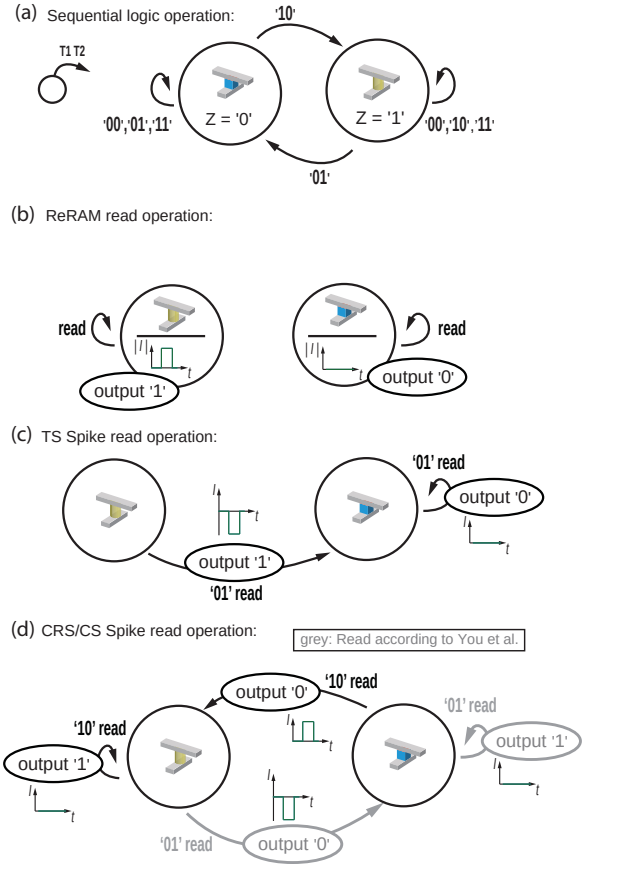

Figure 3. a) Finite state machine (FSM) representation of a memristive device, either basic ReRAM, TS-ReRAM, CRS or CS. Depending on the logic signals at terminal T1 and T2, and the actual device state *Z* (either '0' or '1') the cell switches. For example, T1 = '1,' T2 = '0,' and *Z* = '0' induces a switching from *Z* = '0' to *Z* = '1'. b) For read-out of the ReRAM device a small voltage is applied. A high current level corresponds to the output '1' whereas an output '0' is present if a low current is measured. c) In the case of TS-ReRAM cells a negative write pulse is applied for read-out. The presence of a current spike corresponds to output '1' and the absence corresponds to output '0'. d) For the read-out of CS/CRS cells the same FSM as for the logic operation applies. Here '10' read means T1 = '1' and T2 = '0' while '01' read means T1 = '0' and T2 = '1'. In common memory and CRS-logic read operations use only '10' read. When using the logic concept of You et al. (gray color) also negative read-out can be performed for CS/CRS cells. In both cases, the presence of a current spike is interpreted as output '0' and the absence of a current spike reflects the output '1'.

Note that read-out is not part of the actual logic operation since the final result is directly stored as state *Z* in the device. To read-out the device state *Z*, in case of basic ReRAM cells a small read voltage is applied and the corresponding current flow is measured (Figure 3b). Here, a high current corresponds to '1' whereas a low current means '0'. For TS-ReRAM either a non-destructive read-out, which uses a voltage $V_{TS,1} < V < V_{R,Set}$ for current level evaluation, or a destructive spike read-out scheme can be applied, similar to the spike read in CRS devices.[27] In this work the destructive read-out is used, since it is simpler to implement. Note that for this read operation also a negative write pulse is used (Figure 3c). Here the presence of a spike means '1' and the absence '0'. In terms of CRS and CS devices a voltage $V > V_{th,2}$ (corresponding to a positive write pulse) is applied and the occurrence of a current spike is measured (so-called '10' read in Figure 3d). In contrast to the TS-ReRAM spike read scheme here the presence of a spike means '0' whereas the absence of a spike means '1'. When using also '01' read (corresponding to negative write pulse), one can directly implement XOR and XNOR functions according to You and co-workers.[36] Note that the device state in this logic concept is interpreted depending on the read-out. Thus, the read-out procedure is a conditional operation, i.e., whether the '10' or '01' read is conducted depends on the logic operation itself and the input variables.

4. Measurements of IMP- and AND-Function According to CRS-Logic

For each of the five types of cross-point junction devices the IMP and AND functionality are exemplified using the CRS-logic. The remaining 12 two input logic functions of a CRS-ECM device can be found in the Supporting Information. To achieve each of the 14 two input logic functions sequences of signals at both terminals need to be applied. All logic operations are performed using a single unit cell. All logic functions need to start from a defined state, since the behavior of the devices depends also on the device state. The AND and IMP functions in CRS-logic start with the '1' state. Thus, the first step is an initialization step (marked by a gray background color in **Figures 4–6**) that sets the device state to '1'. This initialization step is followed by two logic steps (yellow and orange background color) for the AND function. In these two steps terminal 2 is set to '1' (high potential). The signal at terminal 1 is set in the first step to p and in the second step q is applied. After the logic steps the result is stored in the device and can be read out. The result of the IMP logic function is obtained after one logic step (yellow). In this step q is applied to terminal 1 and p to terminal 2. After these logic steps the result is verified by a read-out.

To conduct these schemes the pulse length and height need to be adjusted for every considered device, so that the devices always end up in defined resistive states after switching had occurred. If a short pulse length is chosen and signals are applied at both terminals that are unequal zero, then high capacitive spikes are measured. These spikes are an inherent feature of the used measurement setup. Note that the intrinsic switching speed of ReRAM devices was shown to be lower than 200 ps, thus fast logic-in-memory operations are feasible.[39] Here, the pulse lengths were chosen in order to visualize the actual logic operation best for the considered prototypical devices.

In Figure 4a,b, the measurement of AND and IMP functions of the BRS-VCM device are depicted using the above described scheme. Note that the pulse heights at both terminals are different. This is a requirement for the BRS-VCM

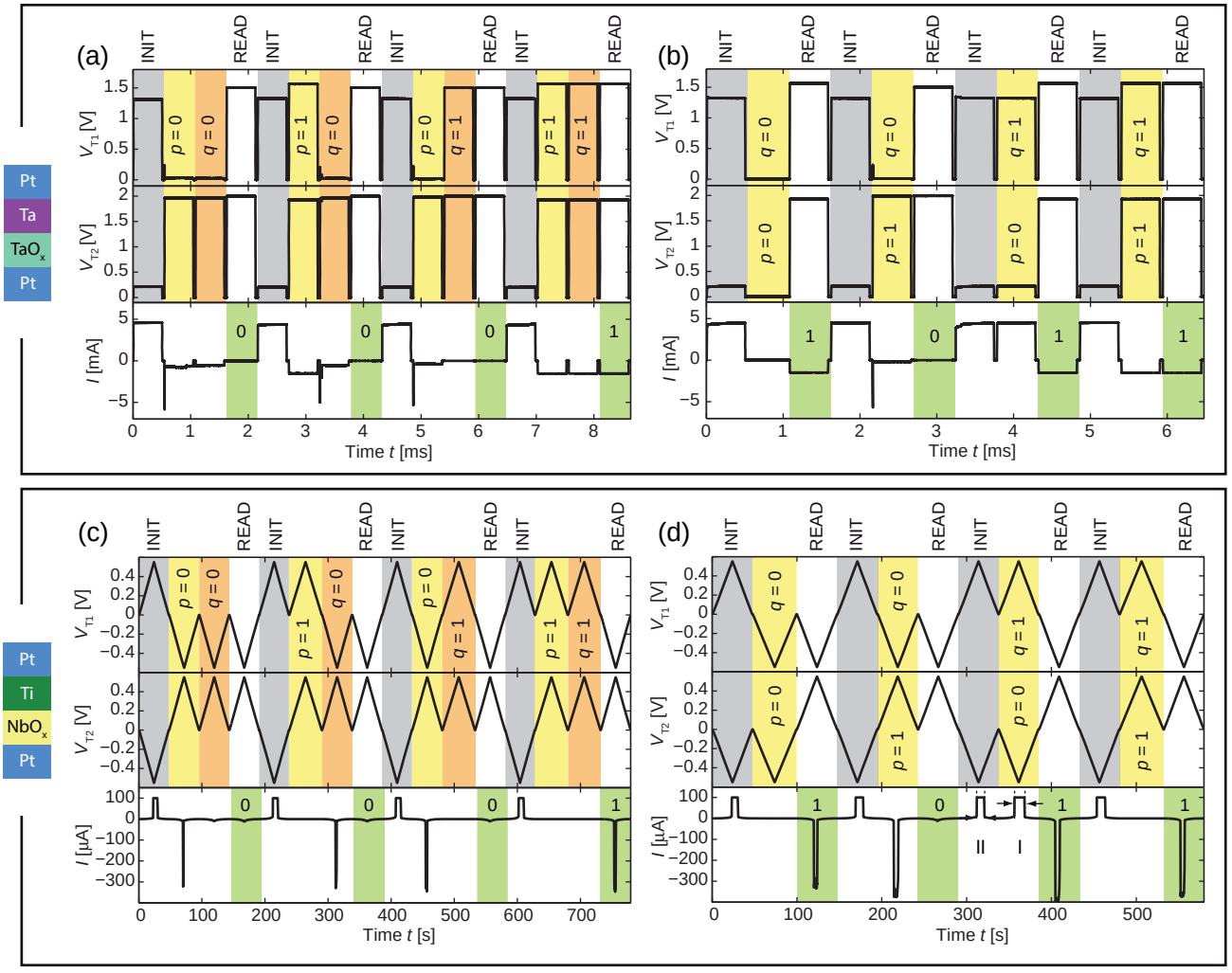

Figure 4. BRS-VCM pulse measurement of the a) AND function and b) IMP function. TS-ReRAM sweep mode measurement of the c) AND function and d) IMP function. In d) I marks the larger current window in the case when the ReRAM was in the LRS and II marks the narrower current window in the case when the ReRAM was in the HRS. For definition of T1 and T2 compare Figure 1.

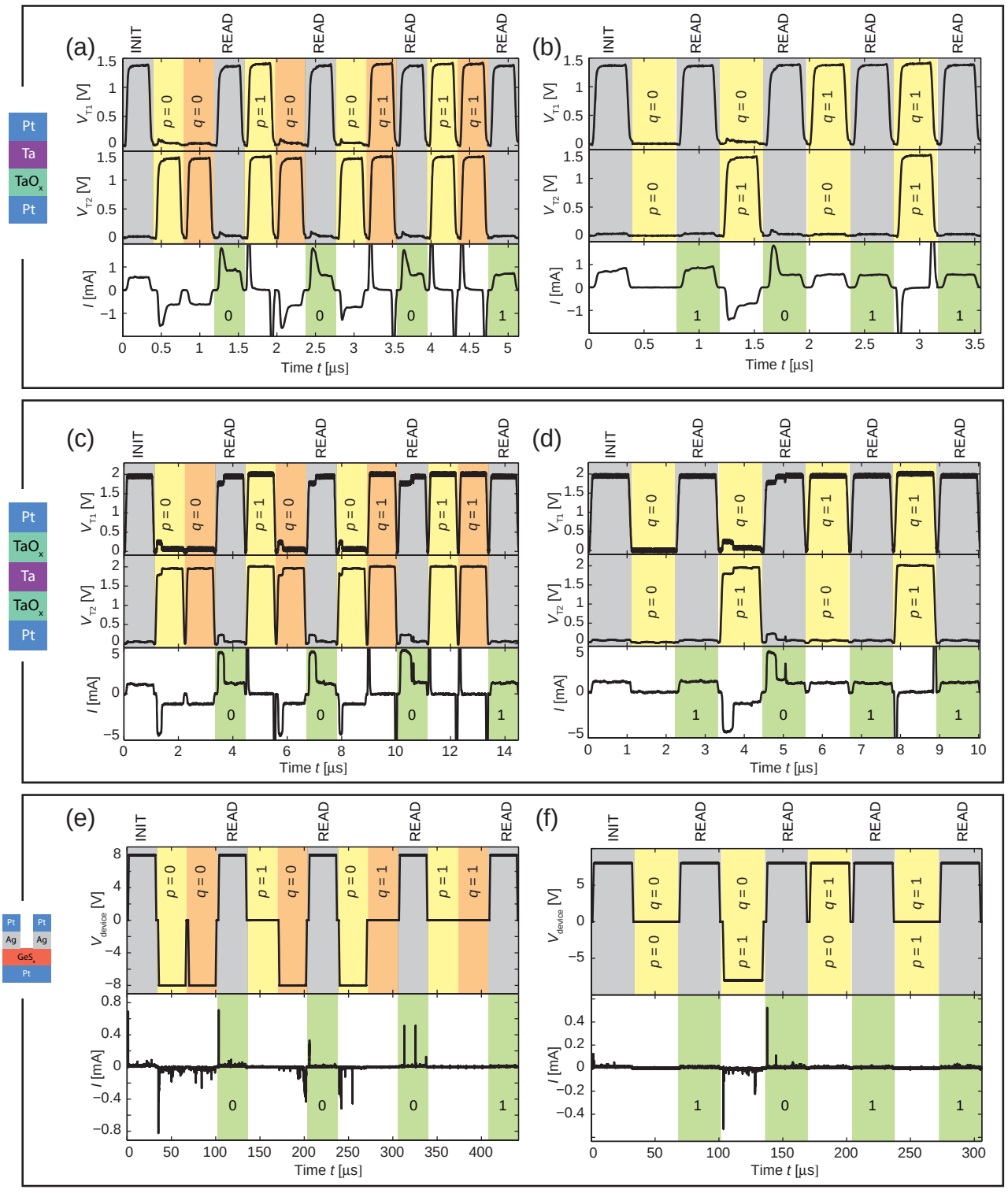

Figure 5. Measurements of the AND and IMP functions for the CS VCM cell in (a) and (b), for the CRS-VCM in (c) and (d), and for the CRS-ECM cells in (e) and (f), respectively. For definition of T1 and T2 compare Figure 1.

device to receive always similar LRS and HRS states after the switching process. This property of the BRS-VCM device results from the difference of SET and RESET kinetics. The read-out in these measurements is performed by applying the high potential ('11') at both terminals. Thereby, only the difference of both high potentials is effectively applied over the

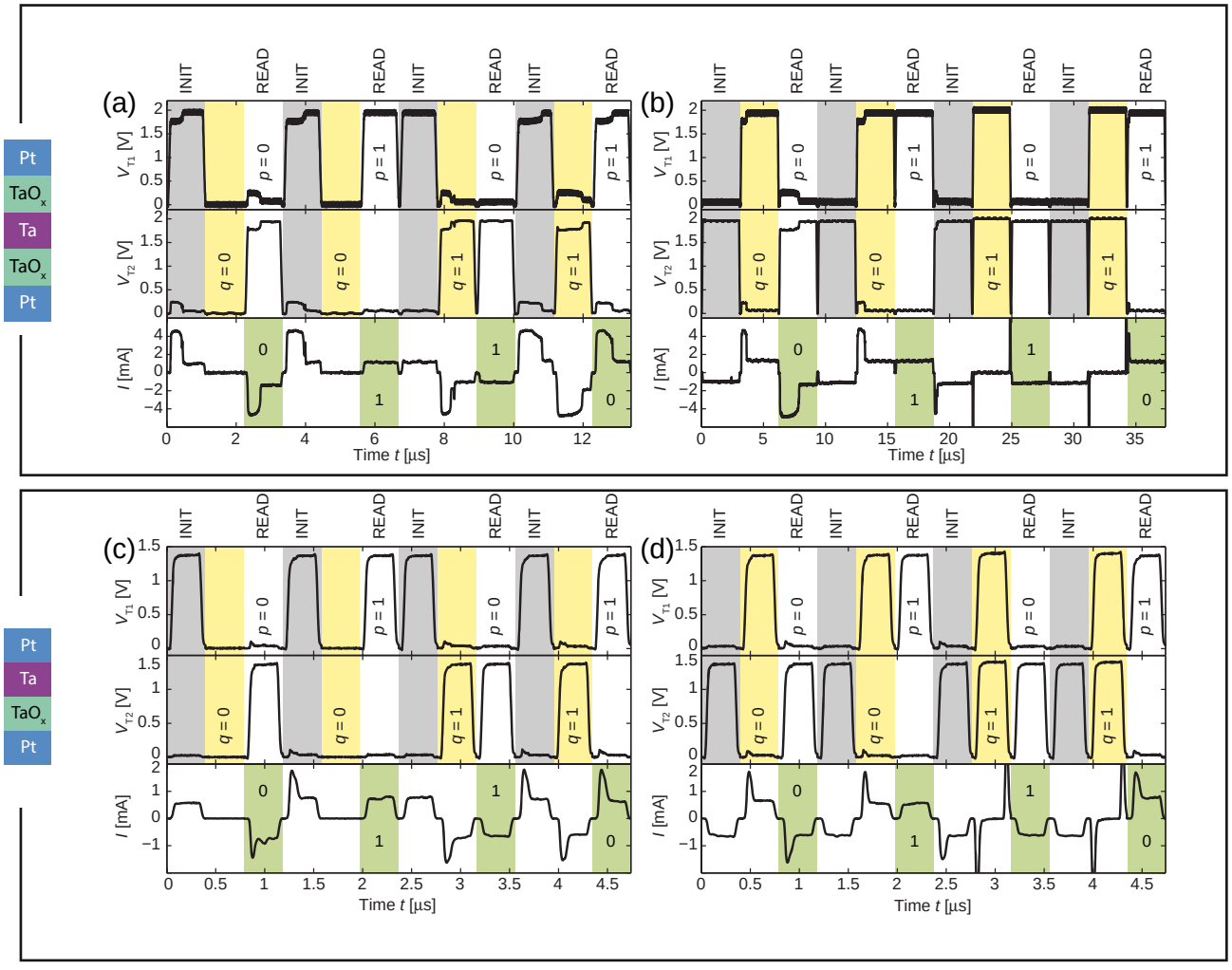

Figure 6. CRS-VCM pulse measurement of the XOR function starting with a) a positive pulse or b) a negative pulse. c) CS-VCM pulse measurement of the XOR function starting with c) a positive pulse or d) a negative pulse. For definition of T1 and T2 compare Figure 1.

device, i.e., –0.5 V. This value is sufficiently small to leave the device state unchanged. If a high current is detected, the result is interpreted as a '1' otherwise as '0'. Since the reading process is nondestructive, the device state is still the result of the logic function. Thus the device has to be initialized before starting the next logic function with a different pair of p and q.

In Figure 4c,d, the measurements of the AND and IMP functions of the TS-ReRAM device are depicted using the above described schemes. This device needs a current compliance for the SET process. Since the used measurement setup cannot provide a current compliance in pulse mode, the measurements were done in sweep mode. In this mode $+V/2$ represents a logical '1' and $-V/2$ a logical '0'. A destructive read-out is used for these measurements since it is easier to realize than a nondestructive read-out.[40,41] The destructive read-out is a simple negative writing sweep. For negative voltages no current window is detected if the ReRAM is in the HRS. In contrast, if the ReRAM is in the LRS, a current window prior to the RESET is observed. Thus, if a current spike is detected the device was in the '1' state otherwise the device was in '0' state. After this read-out step the device is in the '0' state. Since the AND and IMP functions need to start in the '1' state, the cell needs to be initialized afterward. The IMP function measurement also highlights the determining effect of the ReRAM part. If the ReRAM part is in the LRS (case I in Figure 4d), a considerable current flows through the device and the voltage drop at the TS is large. Consequently, the TS switches earlier to the ON state and thus, a wide current window is observed. In the second case, the ReRAM part is in the HRS (case II in Figure 4d). In consequence, less current flows through the device and the voltage drop over the TS is lower, resulting in a smaller current window, since the TS switches to the ON state only if the ReRAM switches to LRS, too.

In Figure **5** the measurements of the AND and IMP functions of the CS-VCM, CRS-VCM, and CRS-ECM devices are depicted using the above described scheme. Due to their similar I–V characteristic (cf. Figure 2) the measurements are performed in the same manner. The read-out is performed using a '10' spike read. If a current spike occurs, the device state was a '0' otherwise it was a '1'. Since the read-out step is destructive and switches the device in the '1' state no initialization step needs to be performed for the next operation.

In the CRS-ECM measurements in Figure 5e,f the difference signal T1 – T2 is applied at the left electrode while GND is applied to the right electrode (see Figure 1d). As the measurements indicate sometimes more than one current spike occurs in the switching step. This behavior can be caused by the polarity-independent RESET operation that can occur for LRS less than 12.9 kΩ.[42] Thus, it is most likely that the device switches back and forth between the LRS/HRS and LRS/LRS before it passes over to HRS/LRS.

5. Measurement Results of the XOR Function

The logic concept used in the previous section shows that only 14 of 16 two input Boolean logic functions are feasible with one ReRAM device.[25] Later You et al. presented an extended concept that enables all 16 two input Boolean logic functions, also including XOR/XNOR, with one $BiFeO_3$:Ti/$BiFeO_3$ device using a conditional read-out.[36] In this logic concept all 16 two input Boolean logic functions can be implemented in three steps by using one ReRAM device. As previously mentioned, all logic functions in this advanced logic concept need to start from a defined device state. So the first step is always an initialization step. It is followed by one logic step and a conditional read-out step. As the conditional read depends on the input variables this step could also be considered as a second logic step. The state after the read-out is undefined, so the next operation must start with an initialization step again.

This logic concept can also be adopted for CRS and CS devices. If a current spike in the reading step is detected regardless of the used read voltage polarity, the read-out information is defined like before as a '0'. If no current spike occurs, the read-out information is interpreted as '1'. For each of the two aforementioned types of cross point junction devices the XOR functionality is exemplified starting either with a positive or a negative initialization step. The measurements of the XNOR functionality starting either with a positive or a negative initialization step can be found in the Supporting Information.

In Figure 6a,c, the measurements of the XOR function starting with a positive pulse of the CS-VCM and CRS-VCM devices are depicted. In this case the first step is an initialization in the '1' state ('10'). Afterwards the low potential is applied to terminal T1 and *q* is applied at terminal T2. Concluding the operation the conditional read-out is performed as a function of *p*. If *p* is a logical '1', a positive read-out ('10') is performed otherwise a negative read-out ('01') is used. If a current spike is detected in this read-out step, the result of the logic function is interpreted as a '0'. Otherwise the result is interpreted as a '1'. In Figure 6b,d the measurements of the XOR function starting with a negative pulse of the CS-VCM and CRS-VCM devices are depicted. In this case the first step is an initialization to the '0' state ('01'). Afterwards the high potential is applied to terminal T1 and *q* is applied to terminal T2. Concluding the operation the conditional read-out is performed as a function of *p*. If *p* is a logical '1' a positive read-out ('10') is performed otherwise a negative read-out ('01') is used.

A major advantage of the extended logic concept is that all 16 two input Boolean functions are feasible with a single device in three cycles. Therefore it should be easier to achieve more complex functions like an adder or multiplier. But the requirements to the amplifiers are growing in this logic concept, due to the fact that read-out can be performed in the positive and negative direction. Also there is less space for cycle count optimization. Since the conditional read-out changes the device to an unknown state the next operation always needs an initialization step. Moreover, the final result is achieved during the conditional read-out. Thus the read-out needs to be considered as an inherent part of the logic operation and the result has to be written back to store it. Parallel calculations are therefore difficult to realize, since every device needs a conditional read-out, i.e., different signals are needed at the wordline and bitline of the crossbar array.

In addition a standard read-out scheme needs to be defined, either the positive read-out ('10') or the negative read-out ('01') to enable normal memory operation in this concept. Otherwise the memory content can be misinterpreted since a stored '1' is interpreted as a '1' if a positive read-out will be used whereas it will be interpreted as a '0' for a negative read-out.

6. Comparison of Cross-Point Devices in Terms of Logic Operations

The requirements for cross-point devices that are used as logic elements differ from pure memory applications. The device endurance is much more important when implementing logic-in-memory concepts. Note, for general purpose logic operations a minimum endurance of up to 10^{17} cycles is required. However, depending on the applications logic operations will be conducted less frequently, e.g., memory intensive computing tasks, so more than 10^9 cycles would be sufficient. Second, the ratio of read to write operations is very different in memory and logic applications. In memory applications the read to write ratio is often more than 100, whereas in logic operations it is less than 0.5 in general.[25] Thus, the reliability of the bipolar write operations is even more important for logic applications. Third, device retention is less important for logic applications since the used cells are often rewritten during the logic operations. For both, memory and logic applications, the selectivity of the devices is the key figure of merit determining the maximum array size, and thus the ReRAM memory to CMOS periphery ratio. For a half select scheme, the selectivity is defined as $NL = I(@V_{read})/I(@1/2V_{read})$.[43]

In the following paragraphs the suitability of available ReRAM-based cross-point elements is discussed with respect to 1) the endurance, 2) the reliability of the bipolar switching mode, and 3) the selectivity.

First, the properties of basic, ECM-type and VCM-type, ReRAM cells are highlighted. An endurance above 10^{10}[2] switching cycles was shown for ECM devices whereas VCM devices offer up to 10^{12}[3] switching cycles. In arrays up to 10^6 cycles were demonstrated for both types,[44] which is much below 10^{17} cycles. Thus improving the endurance is one of the most crucial challenges of today's available ReRAM cells. Concerning the reliability of bipolar operation mode, ECM devices should be operated in a low current range to avoid any polarity-independent RESET. In VCM devices another kind of failure mechanism is predominant, namely with the occurrence of

unintended CS-type switching.[45] In general, the composition of the VCM device stack influences the vulnerability to this kind of failure mechanism and can be reduced by optimizing the layer thicknesses, for example. Typically, ECM devices show a high R_{OFF}/R_{ON} ratio in the range about $\approx 10^6$ whereas VCM devices typically offer lower ratios of up to 10^3.[4,46] Improving the R_{OFF}/R_{ON} ratio of the VCM cells by further device engineering may result in a tradeoff between large R_{OFF} values and switching speed. Nevertheless, for the array compatibility the R_{OFF}/R_{ON} ratio of BRS devices is less crucial than the selectivity, which is only $NL = 2$ for ReRAM devices offering linear LRS and HRS branches.

Note that a large array size cannot be reached with such devices,[47] so a certain nonlinearity needs to be added to the devices. Although some VCM devices offer inherent nonlinearity in the LRS branch [30,43] the selectivity is still low with $NL < 10$ for most devices. However, $NL > 50$ has also been observed in area-type switching VCM devices but the retention of those devices is not sufficient.[48] Higher values can be obtained when using a selector, i.e., a 1S1R cell (1 selector 1 ReRAM device).[49] When using a selector the R_{OFF}/R_{ON} ratio becomes a relevant value, since the R_{OFF}/R_{ON} of the total 1S1R stack is reduced when adding a selector. Since CRS-logic is feasible for BRS-VCM devices it will also work for any kind of 1S1R device.

An additional serial selector can be avoided by applying a selectorless configuration. For example, the TS-ReRAM device offers a high selectivity ($NL > 100$[50] and a very high R_{OFF}/R_{ON} ratio in the ON-window, thus the array compatibility is high. However, typically this device needs higher write voltages than a single cell due to the fact that part of the voltage drops at the TS and the other at the ReRAM (voltage divider). Moreover, the possibly lower switching speed of the TS could limit the overall device performance. In terms of save bipolar operation mode, the reliability of TS must be improved. For the read-out one can use a simple destructive read-out by applying a negative write pulse and evaluating whether a current spike occurs or not. To achieve a nondestructive read-out the ON-window has to be accessed very precisely to avoid unintended switching. Since this range is very narrow, the variability of the device and the voltage level has to be very small which is difficult to achieve. Furthermore the smallest feasible feature size has not been evaluated until now. The best endurance data for this type of device is more than 1000 cycles.[50]

CRS devices require also higher switching voltages than pure ReRAM cells, since the device consists of two antiserially connected ReRAM devices. The selectivity of CRS device is strongly depending on the considered ReRAM devices, i.e., R_{OFF}/R_{ON} ratio and so a matter of device engineering. CRS-VCM devices in general offer smaller R_{OFF}/R_{ON} ratio and a wider ON-window but show more stable operation.[35] However the selectivity of TaO_x-based CRS devices was shown to be $NL > 60$,[51] whereas the best endurance was shown to be more than 10^6 cycles.[35] ECM devices normally show a higher R_{OFF}/R_{ON} ratio and a very sharp current spike, but stable operation is an issue in those devices. To achieve a stable CRS operation the occurrence of unintended polarity-independent RESET has to be avoided. Thus, a low current operation has to be guaranteed if the CRS is in the LRS/LRS state, which has not been demonstrated yet.

Complementary switching is only available in VCM cells. CS-VCM devices offer similar switching voltages compared to a single cell since they have the same layer structure (cf. Figure 1). An endurance of more than 10^3 cycles and a selectivity $NL > 10$ was shown for HfO_x-based device,[38] but a selectivity $NL > 100$ was also reported for an $SrTiO_x$-based CS device.[52] If the R_{OFF}/R_{ON} ratio and the voltage levels ($V_{th,1}$ and $V_{th,3}$) can be improved by device engineering, the selectivity might be improved, too. Moreover, the reliability of the regular CS switching is an issue, e.g., a common failure mechanism in those devices is the occurrence of conventional bipolar resistive switching.

7. Conclusion

In this paper, we proved by means of electrical measurements the feasibility of logic-in-memory operations using 1) BRS-VCM cells, 2) TS-ReRAM cells, 3) CRS-VCM cells, 4) CRS-ECM cells, and 5) CS-VCM cells. In principle any bipolar resistive switching material, either ECM-type or VCM-type, can be used. When using CS or CRS cells 16 Boolean functions are feasible with a single device. In terms of array compatibility TS-ReRAM, CS-ReRAM, and CRS are all well suited candidates for implementing logic-in-memory functionality.

8. Experimental Section

Device Fabrication—BRS-VCM, CS-VCM, and CRS-VCM: A thermal oxidized 4″ Si wafer with a Ti(5 nm)/Pt(30 nm) thin film is used as a substrate, where Ti is a adhesion layer. Next, the BE structure is transferred into the Ti/Pt layers with photolithography and reactive ion beam etching (RIBE). Subsequently, the switching layer Ta_2O_5, Ta (TE) and Pt (capping layer) for the BRS-VCM and the CS-VCM, whereas the switching layer Ta_2O_5 (bottom active layer), Ta (middle electrode), Ta_2O_5 (top active layer), and Pt (TE) for the CRS-VCM were deposited at room temperature by a sputtering process. The Ta_2O_5 layer has been deposited with a reactive sputtering technique with a Ta target under the gas mixture of Ar (77%) and oxygen (23%) and the Ta layer deposition has been carried out using only Ar gas at the chamber pressure of 2.3×10^{-2} mbar and with the radio frequency (RF) power of 116 W for the CS-VCM and the CRS-VCM devices, whereas a RF power of 232 W was used for the BRS-VCM device. The Pt layer was deposited with a DC sputtering process at a chamber pressure of 1.4×10^{-2} mbar and a power of 374 W. In the final step, the Ta_2O_5 layer(s), Ta and the top Pt layer are patterned by photolithography and RIBE. For the BRS-VCM device, the layer sequence consists of 5 nm Ta_2O_5/13 nm Ta/25 nm Pt, whereas, the layer stack for the CS device is 5 nm Ta_2O_5/5 nm Ta/25 nm Pt. For the CRS device the layer sequence consists of 5 nm Ta_2O_5/10 nm Ta/5 nm Ta_2O_5/25 nm Pt.

CRS-ECM: In this study, the CRS-ECM devices were fabricated as two antiserially connected Ag/GeS_x/Pt (being Ag the active and Pt the inert electrode) electrochemical metallization cells (ECM)[53] with an accessible common middle electrode.[37] The middle electrode was produced as a 50 nm thick and 2 µm wide Pt finger and acted as the inert electrode in the two ECM cells. The active electrodes were fabricated as 50 nm thick and 2 µm wide Ag fingers perpendicular to the middle electrode, resulting in a cross-point area of 4 μm^2. The Ag electrodes were covered with a 50 nm film of Pt for protection. A sputtered 70 nm thin film of GeS_x with an S to Ge ratio of 2.2 was used as the solid electrolyte between the middle electrode and the two active electrodes and produced according to the procedures published before.[54] The

middle electrode at the bottom of the stacks was structured by ion beam etching, whereas the contact hole in the GeS_x thin film and the topmost active electrodes were structured by a lithographical lift-off process.

TS-ReRAM: The TS-ReRAM devices investigated in this study consisted of a 10 nm thin niobium oxide layer sandwiched between a platinum and a titanium electrode. The nanocrossbar devices of (100×100) nm^2 size were fabricated on thermal oxidized Si wafers starting with a sputtered Ti (5 nm)/Pt (25 nm) BE. The structures were fabricated by means of UV nanoimprint lithography and RIBE. The 10 nm thick Nb_2O_5 film was grown by atomic layer deposition (ALD) at 275 °C using ^{t}BuN = Nb(NMEt)$_3$ and O_3 as the metal and oxygen source, respectively. The TE of 5 nm Ti/25 nm Pt was deposited by e-beam evaporation on the as-grown amorphous Nb_2O_5 film. Then the TE pattern was defined by e-beam lithography. Afterwards, the TE metal and the Nb_2O_5 film were structured by means of RIBE. Details on the ALD[55] and nanocrossbar device fabrication processes[56] are described elsewhere.

Electrical Measurement: The needed forming procedure of the considered devices was done using either a computer controlled Keithley 2636A or a Keithley 4200 SMU. The latter was also used for the sweep-mode measurements whereas for the pulse measurements two Keithley 4225 PMUs with associated remote amplifiers were used. To perform the measurement the two device terminals T1 and T2 are connected by probing needles to the Keithley measurement system.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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